Ultra-Coins等の活動報告

情報科学類3年　高橋玉緒

Ultra-Coinsに4月ごろ加入

1. はじめに- how works an MRAM

- Magnetic Tunnel Junction (MTJ) is the core of MRAM

  It Two magnetic layers:
  - **Reference layer(s) (RL)**: fixed magnetization is stable.
  - Thin insulating **tunnel barrier** (e.g. MgO)
  - **Free layer (FL)**: storage layer, magnetization can switch (up/down

- **Read (Non-destructive): TMR**

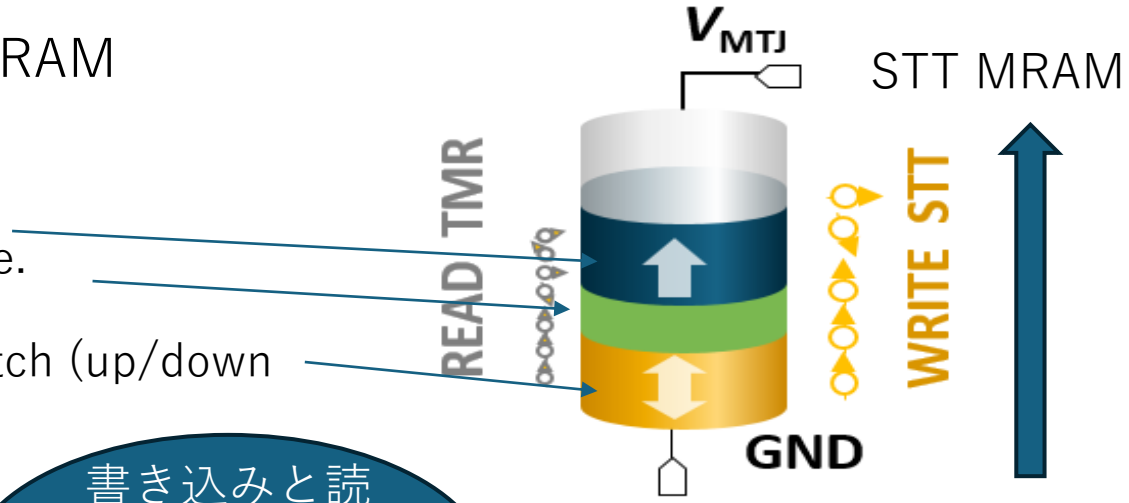
  Apply a small voltage across the MTJ.

  Resistance depends on relative orientation RL-FL :
  - Low R(Parallel) → Bit is “0”
  - High R(Anti parallel) → Bit is “1”

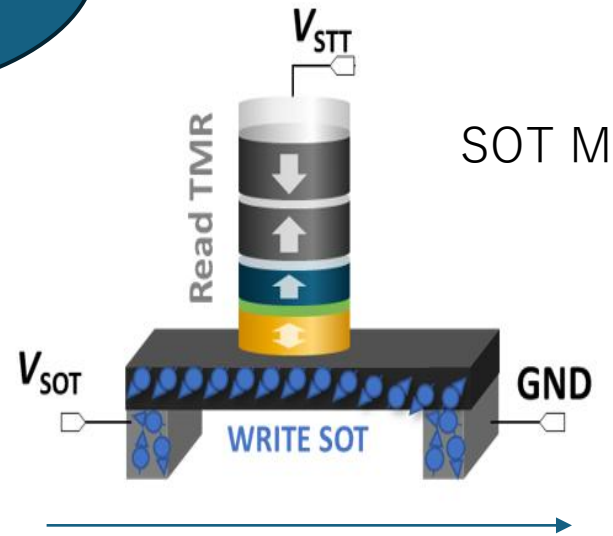
  TMR = (Rap-Rp)/Rp

- **Write (ex. Spin-Transfer Torque and Spin orbit torque):**

  When a spin current pass through, it torques Free layer. It can switch the direction of the magnet when large enough
  - STT: spin current created by magnetization
  - SOT: spin current created by non magnetic signal via spin orbit interaction



書き込みと読み出し経路を分けることで耐久性向上

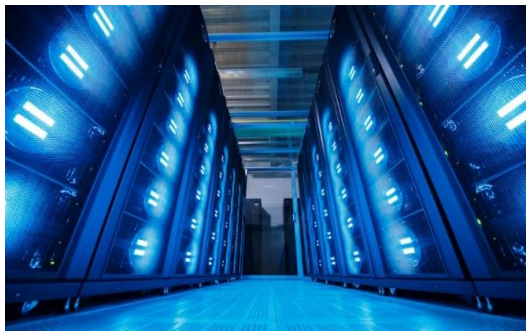


SOT MRAM

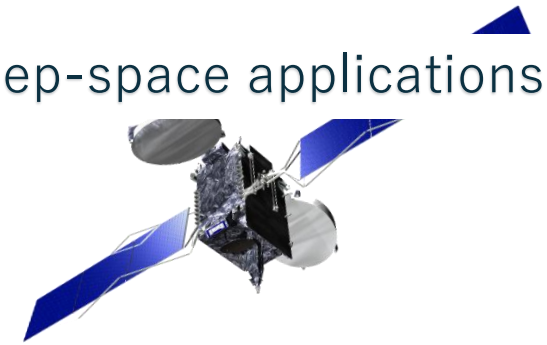
Interest to study SOT-MRAM at cryogenic temperatures?

- Device reliability changes under different temperatures.
- Understanding **TMR**, **coercive field**, and **stability** at low T is crucial.
- Important for:
  - Industrial adoption
  - **Cryogenic computing** & **quantum tech, space satellite**

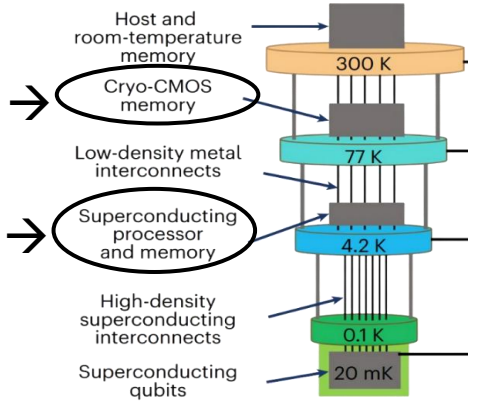
High-performance computing



Deep-space applications



Quantum computing



Alam, S. *et al.* Cryogenic memory technologies. *Nat Electron* **6**, 185–198 (2023)

なぜSOT-MRAM？-取り組み期間：2026年4月~

Why SOT-MRAM?

- **High Density: Small cell size allows for larger cache capacity within the same chip area compared to SRAM.[2]**
- **Non-Volatility: Zero leakage power enables energy-efficient "normally-off" computing.[1][2][3]**
- **High Speed: Offers faster switching speed than STT-MRAM, making it suitable for L2/L3 caches.**

Feature	SRAM	DRAM	SOT-MRAM
Non-Volatility	No	No	Yes
Cell Size F^2	Large (~146)	Small (~6)	Medium (~46–60)
Leakage Power	High	High (Refresh)	Near Zero
Read Latency	Very Fast (<1 ns)	Slow (~30 ns)	Fast (~3 ns)
Write Latency	Very Fast (<1 ns)	Slow (~30 ns)	Fast (~5 ns)
Endurance	Unlimited (10^{16})	Unlimited	High (>10^{12})

Table 1　Comparison between SRAM, DRAM and SOT-MRAM[1]

実験方法

L2, 3はL1よりも速度が落ちても容量が増える利点が大きい

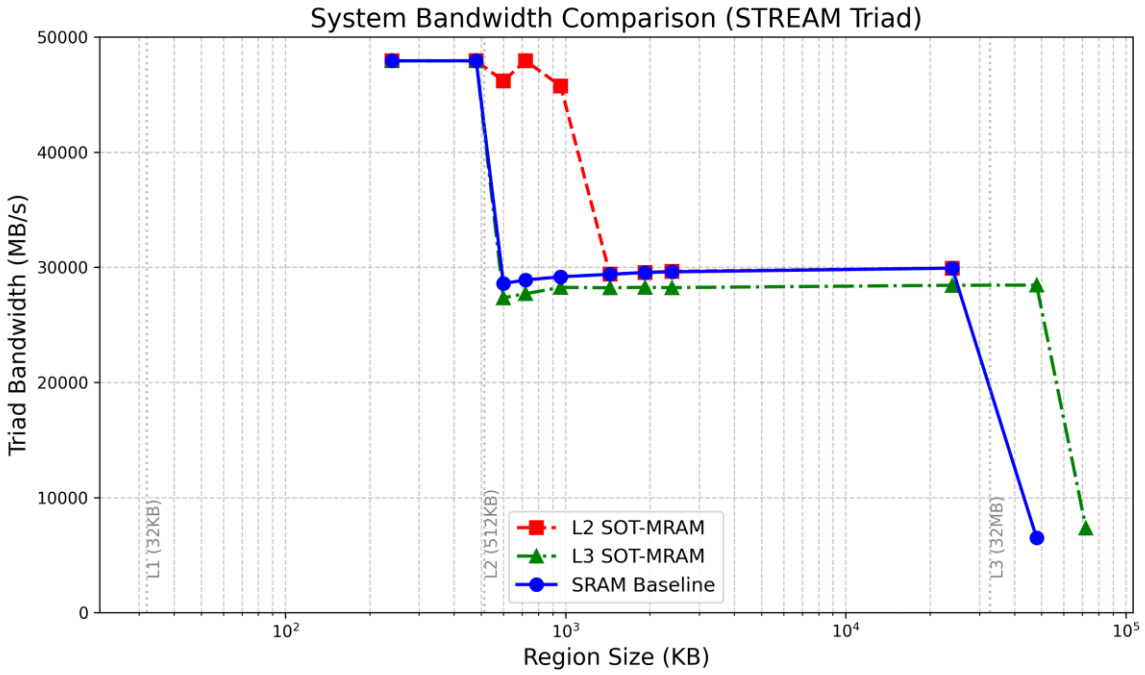
Simulation Environment

- gem5: Cycle-accurate full-system simulator for architecture modeling.
- STREAM: Benchmark for measuring sustained memory bandwidth.
- In this study, we simulated a 4-core DerivO3CPU architecture executing OpenMP parallel workloads, including SOT-MRAM for L2 and L3 caches using gem5 and compared the outputs against a baseline.
- Main Memory: The DDR3 configuration (12.8 GB/s peak) gives ~10 GB/s sustained bandwidth (~80% efficiency)
- Higher Density: The compact nature of SOT-MRAM's 3-terminal structure, compared to the conventional 6-transistor (6T) SRAM.[3]
- →We simulated the SOT-MRAM configuration with double the capacity of the SRAM baseline.

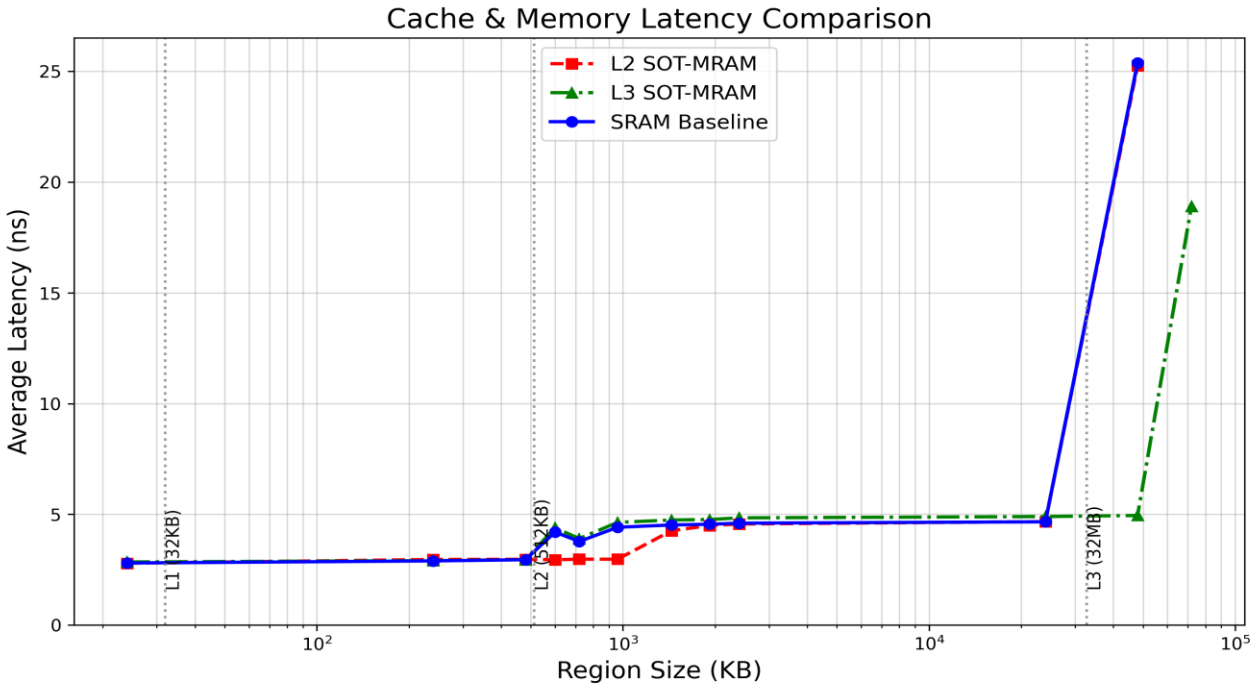
Level	SRAM Baseline Configuration	SOT-MRAM Configuration
L1	32KB I/D(SRAM)	32KB I/D (SRAM)
L2	512 KB (SRAM)	1 MB (2x SOT-MRAM)
L3	32 MB (SRAM)	64 MB (2x SOT-MRAM)

Table 2　Cache size configuration

結果



高い帯域幅を保っている



低いレイテンシの区間が拡張されている

まとめ

- SOT-MRAM(磁気メモリ)の研究は今でも行われている
  - 特に、L2, 3キャッシュやモバイルのデバイス
- SRAMに比べて端子が少ないため高密度で集積できるのが利点

- 今後：詳細なモデリングを続ける
  - 現在はR/Wのレイテンシを分割して複数条件下で計測中
  - HPIコアを使ってARMノードで実験
  - できれば極低温での様々なパラメータ(TMR, 保磁力 etc)の温度依存性を反映させたい
  - 不揮発であることの利点は本当にあるのか、消費電力の検証
    - それもアプリケーションによるので、スイートスポットとなるアプリケーションを見つける
- Ultra-Coinsの環境を生かして、
  - Linuxサーバやビルドシステムなど、このトピック周辺のシステム技術にも取り組みながら、コンピュータアーキテクチャへの理解を深めたい
  - メンバーとの交流を通じて、ネットワーク等の知見も深めたい(取り組みについて話すという文化が新鮮)